PRELIMINARY

T-49-19-16

T-49-19-59

# 87C196KB/83C196KB/80C196KB 16-BIT HIGH PERFORMANCE CHMOS MICROCONTROLLER

**87C196KB — 8 Kbytes of On-Chip EPROM**
**83C196KB — 8 Kbytes of Factory Mask-Programmed ROM**
**80C196KB — ROMless**

- 8 Kbytes of On-Chip EPROM
- 232 Byte Register File
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- 2.3 μs 16 x 16 Multiply (12 MHz)
- 4.0 μs 32/16 Divide (12 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- Pulse-Width-Modulated Output
- Four 16-Bit Software Timers
- 10-Bit A/D Converter with Sample/Hold
- HOLD/HLDA Bus Protocol
- 12 MHz Version — 87C196KB12/83C196KB12/80C196KB12
  10 MHz Version — 87C196KB10/83C196KB10/80C196KB10

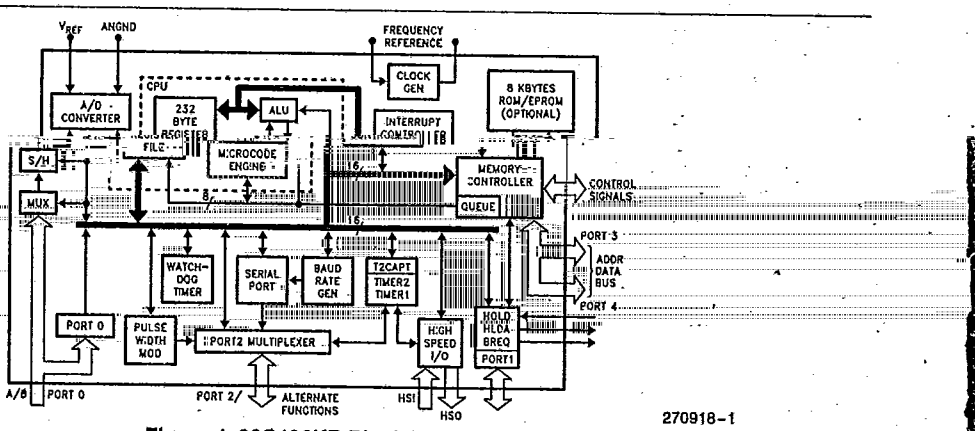
KB 16-bit microcontroller is a high performance member of the MCS®-96 microcontroller family. KB is compatible with the 8096BH and uses a true superset of the 8096BH instructions. Intel's ess provides a high performance processor along with low power consumption. To further reduce ements, the processor can be placed into Idle or Powerdown Mode.

KB has a 232-byte register file and an optional 8 Kbyte of on-chip ROM or EPROM. The ll refer to all of the above products unless otherwise stated.

d and some 32-bit operations are available on the 80C196KB. With a 12 MHz oscillator a 16-bit s 0.66 μs, and the instruction times average 0.5 μs to 1.5 μs in typical applications.

ed capture inputs are provided to record times when events occur. Six high-speed outputs are pulse or waveform generation. The high-speed output can also generate four software timers or conversion. Events can be based on the timer or up/down counter.

on-chip are an A/D converter, serial port, watchdog timer, and a pulse-width-modulated output




270918-1

**Figure 1. 80C196KB Block Diagram**

tered trademark of Intel Corporation.



October 1990
Order Number: 270918-001

The 80C196K
The 80C196K
CHMOS proc
power require

The 80C196K
80C196KB wi

Bit, byte, wor
addition takes

Four high-spe
available for p
start an A/D

Also provided
signal.

MCS®-96 is a regis

## ARCHITECTURE

The 80C196KB is a member of the MCS® 96 family, and as such has the same architecture and uses the same instruction set as the 8096BH. Many new features have been added on the 80C196KB including:

### CPU FEATURES

Divide by 2 instead of divide by 3 clock for 1.5X performance

Faster instructions, especially indexed/indirect data operations

2.33 μs 16 × 16 multiply with 12 MHz clock (was 6.25 μs on the 8096BH)

Faster interrupt response (almost twice as fast as 8096BH)

Powerdown and Idle Modes

5 new instructions including Compare Long and Block Move

8 new interrupt vectors/6 new interrupt sources

### PERIPHERAL FEATURES

SFR Window switching allows read-only registers to be written and vice-versa

Timer2 can count up or down by external selection

Timer2 has an independent capture register

HSO line events are stored in a register

HSO has CAM Lock and CAM Clear commands

New Baud Rate values are needed for serial port, higher speeds possible in all modes

Double buffered serial port transmit register

Serial Port Receive Overrun and Framing Error Detection

PWM has a Divide-by-2 Prescaler

$\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ Bus Protocol

## PACKAGING

The 87C196KB is available in a 68-pin LCC (windowed) package and a 68-pin PLCC (One Time Programmable) package.

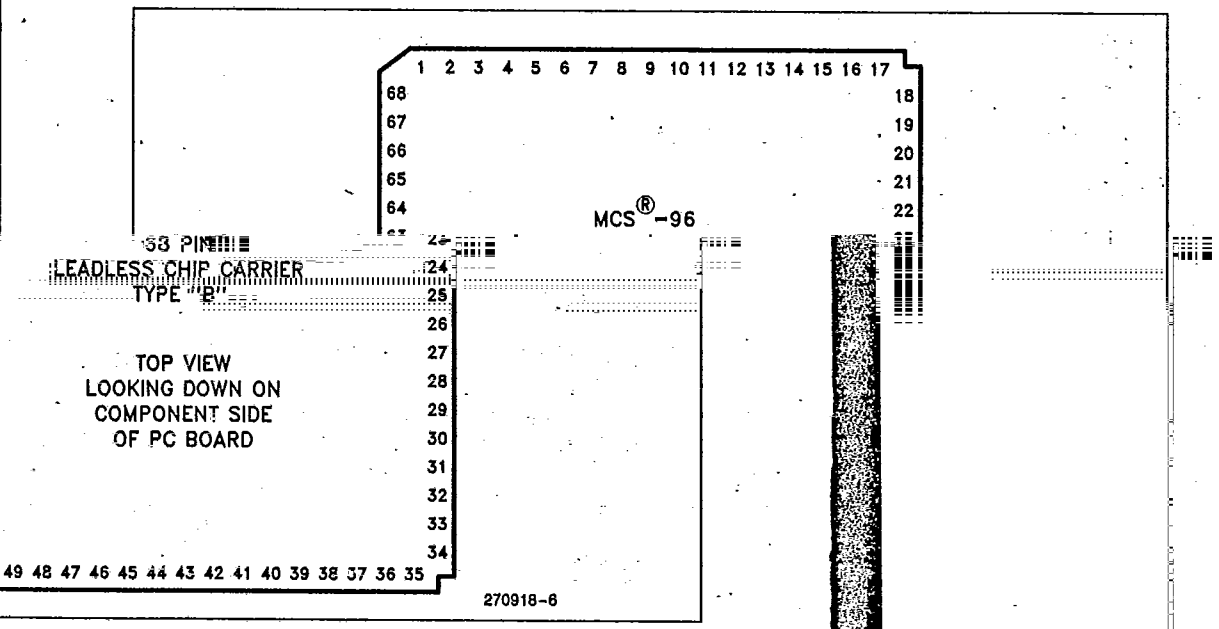
The 80C196KB and 83C196KB are available in a 68-pin PLCC package and an 80-pin QFP package. In addition, the 80C196KB is available in a 68-pin PGA package. Contact your local sales office to determine the exact ordering code for the part desired.

| | LCC | PLCC | QFP | PGA |
|---|---|---|---|---|
| 87C196KB | R87C196KB | N87C196KB | — | — |
| 83C196KB | — | N83C196KB | S83C196KB | — |
| 80C196KB | — | N80C196KB | S80C196KB | A80C196KB |

| PGA | PLCC | Description | PGA | PLCC | Description | PGA | PLCC | Description |
|---|---|---|---|---|---|---|---|---|
| 1 | 9 | ACH7/P0.7 | 24 | 54 | AD6/P3.6 | 47 | 31 | P1.6/$\overline{HLDA}$ |
| 2 | 8 | ACH6/P0.6 | 25 | 53 | AD7/P3.7 | 48 | 30 | P1.5/$\overline{BREQ}$ |
| 3 | 7 | ACH2/P0.2 | 26 | 52 | AD8/P4.0 | 49 | 29 | HSO.1 |
| 4 | 6 | ACH0/P0.0 | 27 | 51 | AD9/P4.1 | 50 | 28 | HSO.0 |
| 5 | 5 | ACH1/P0.1 | 28 | 50 | AD10/P4.2 | 51 | 27 | HSO.5/HSI.3 |
| 6 | 4 | ACH3/P0.3 | 29 | 49 | AD11/P4.3 | 52 | 26 | HSO.4/HSI.2 |
| 7 | 3 | NMI | 30 | 48 | AD12/P4.4 | 53 | 25 | HSI.1 |
| 8 | 2 | $\overline{EA}$ | 31 | 47 | AD13/P4.5 | 54 | 24 | HSI.0 |
| 9 | 1 | $V_{CC}$ | 32 | 46 | AD14/P4.6 | 55 | 23 | P1.4 |
| 10 | 68 | $V_{SS}$ | 33 | 45 | AD15/P4.7 | 56 | 22 | P1.3 |
| 11 | 67 | XTAL1 | 34 | 44 | T2CLK/P2.3 | 57 | 21 | P1.2 |
| 12 | 66 | XTAL2 | 35 | 43 | READY | 58 | 20 | P1.1 |
| 13 | 65 | CLKOUT | 36 | 42 | T2RST/P2.4/$\overline{AINC}$ | 59 | 19 | P1.0 |
| 14 | 64 | BUSWIDTH | 37 | 41 | $\overline{BHE}$/$\overline{WRH}$ | 60 | 18 | TXD/P2.0 |
| 15 | 63 | INST | 38 | 40 | $\overline{WR}$/$\overline{WRL}$ | 61 | 17 | RXD/P2.1 |
| 16 | 62 | ALE/$\overline{ADV}$ | 39 | 39 | PWM/P2.5 | 62 | 16 | $\overline{RESET}$ |
| 17 | 61 | $\overline{RD}$ | 40 | 38 | P2.7/T2CAPTURE/$\overline{PACT}$ | 63 | 15 | EXTINT/P2.2 |
| 18 | 60 | AD0/P3.0 | 41 | 37 | $V_{PP}$ | 64 | 14 | $V_{SS}$(1) |
| 19 | 59 | AD1/P3.1 | 42 | 36 | $V_{SS}$ | 65 | 13 | $V_{REF}$ |
| 20 | 58 | AD2/P3.2 | 43 | 35 | HSO.3/SID3 | 66 | 12 | ANGND |
| 21 | 57 | AD3/P3.3 | 44 | 34 | HSO.2/SID2 | 67 | 11 | ACH4/P0.4 |
| 22 | 56 | AD4/P3.4 | 45 | 33 | P2.6/T2UP-DN | 68 | 10 | ACH5/P0.5 |
| 23 | 55 | AD5/P3.5 | 46 | 32 | P1.7/$\overline{HOLD}$ | | | |

**NOTE:**
1. This pin was formerly the Clock Detect Enable pin. This function is not guaranteed to work. This pin must be directly connected to $V_{SS}$.

**Figure 2. Pin Definitions**




**ure 3. 68-Pin Package (LCC—Top View)**

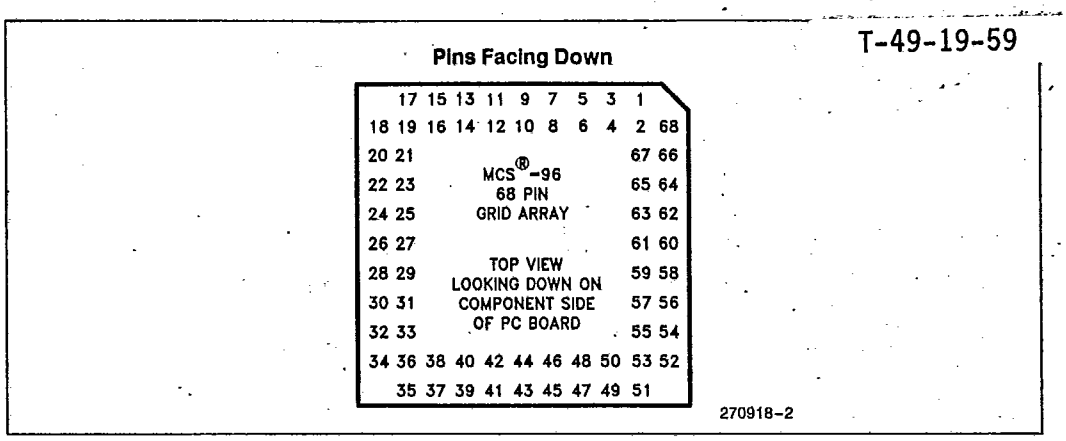



**Figure 4. 68-Pin Package (Pin Grid Array—Top View) 80C196KB Only**

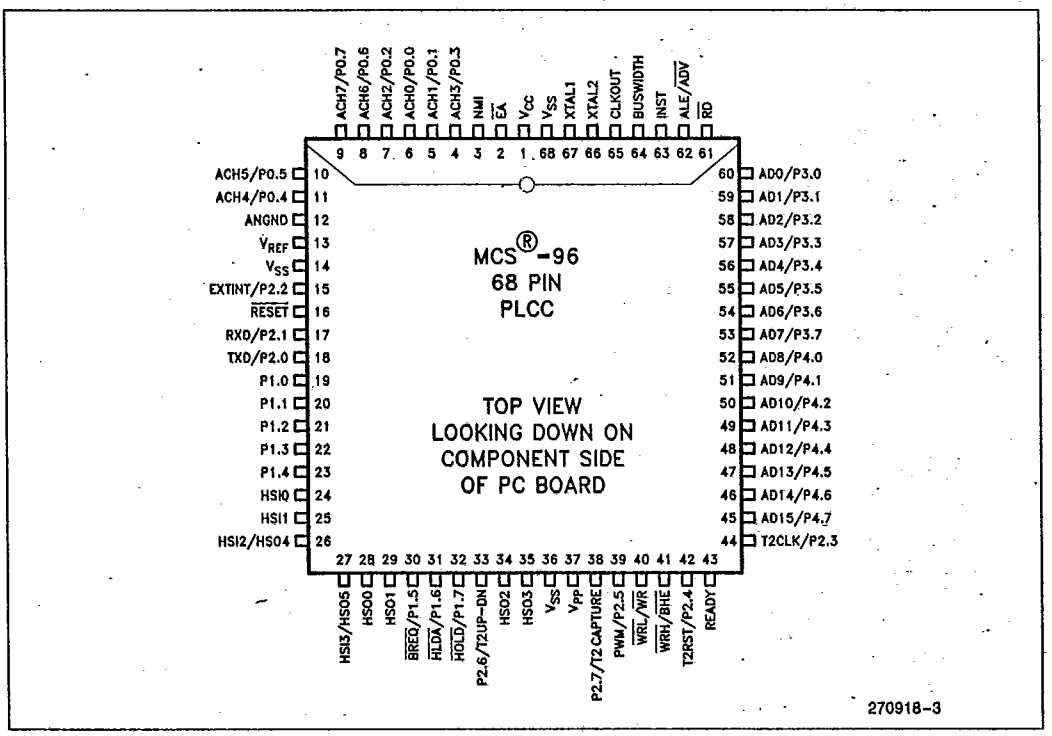
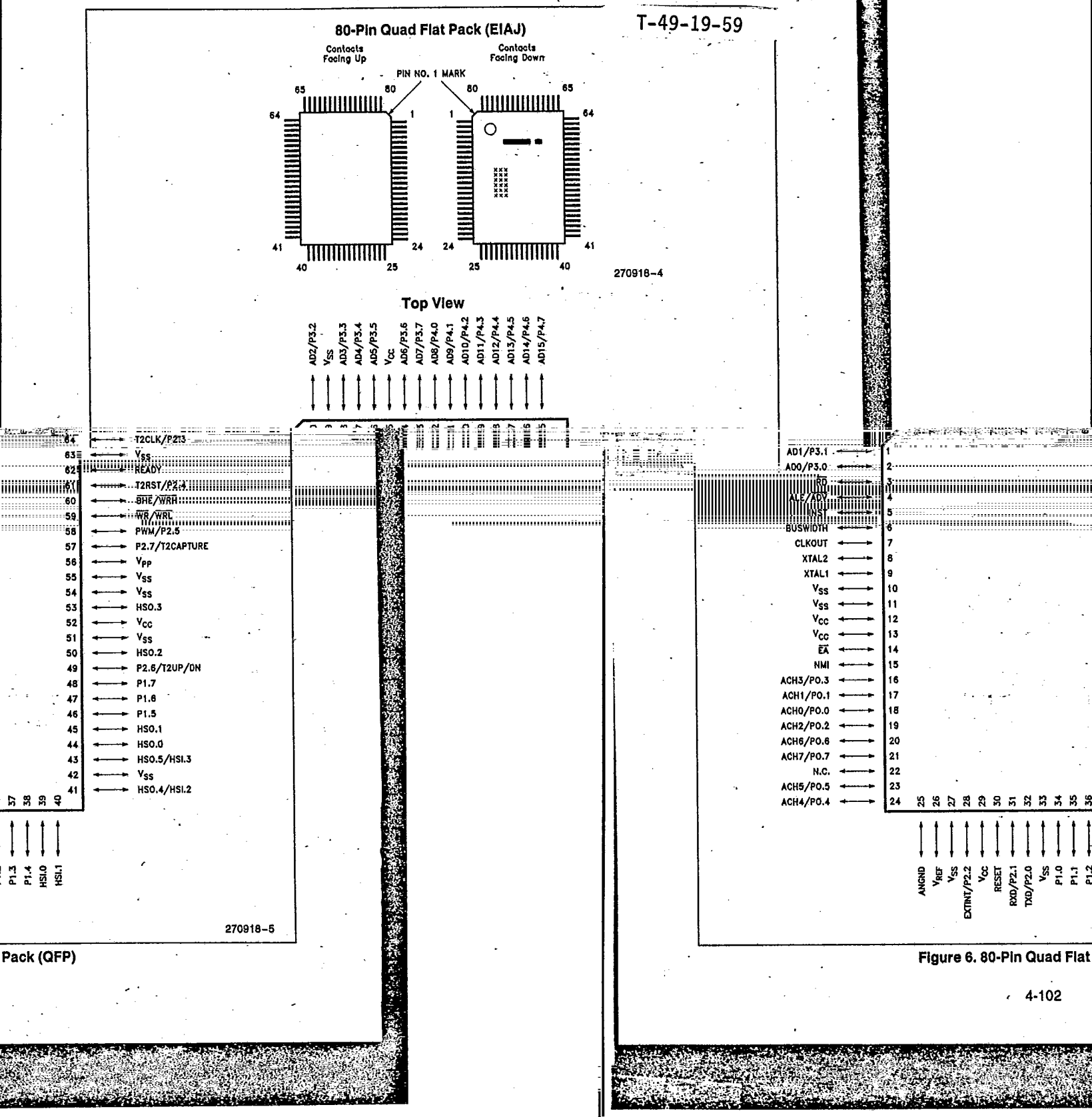



**Figure 5. 68-Pin Package (PLCC—Top View)**




Pack (QFP)

Figure 6. 80-Pin Quad Flat

| Thermal Characteristics | | |
|---|---|---|
| Package Type | $\theta_{ja}$ | $\theta_{lc}$ |
| LCC | 28°C/W | 3.5°C/W |
| PGA | 28°C/W | 3.5°C/W |
| PLCC | 35°C/W | 12°C/W |
| QFP | 80°C/W | |

## PIN DESCRIPTIONS

| Symbol | Name and Function |
|---|---|
| $V_{CC}$ | Main supply voltage (5V). |
| $V_{SS}$ | Digital circuit ground (0V). There are two $V_{SS}$ pins, both of which must be connected. |
| $V_{REF}$ | Reference voltage for the A/D converter (5V). $V_{REF}$ is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function. |
| ANGND | Reference ground for the A/D converter. Must be held at nominally the same potential as $V_{SS}$. |
| $V_{PP}$ | Timing pin for the return from powerdown circuit. Connect this pin with a 1 µF capacitor to $V_{SS}$. If this function is not used, connect to $V_{CC}$. This pin is the programming voltage on the EPROM device. |
| XTAL1 | Input of the oscillator inverter and of the internal clock generator. |
| XTAL2 | Output of the oscillator inverter. |
| CLKOUT | Output of the internal clock generator. The frequency of CLKOUT is ½ the oscillator frequency. It has a 50% duty cycle. |
| RESET | Reset input to the chip. Input low for at least 4 state times to reset the chip. The subsequent low-to-high transition re-synchronizes CLKOUT and commences a 10-state-time sequence in which the PSW is cleared, a byte read from 2018H loads CCR, and a jump to location 2080H is executed. Input high for normal operation. RESET has an internal pullup. |
| BUSWIDTH | Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus. |
| NMI | A positive transition causes a vector through 203EH. |
| INST | Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch. |
| $\overline{EA}$ | Input for memory select (External Access). $\overline{EA}$ equal to a TTL-high causes memory accesses to locations 2000H through 3FFFH to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal to a TTL-low causes accesses to these locations to be directed to off-chip memory. $\overline{EA}$ must be tied low for the 80C196KB ROMless device. |
| ALE/$\overline{ADV}$ | Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$, it goes inactive high at the end of the bus cycle. $\overline{ADV}$ can be used as a chip select for external memory. ALE/$\overline{ADV}$ is activated only during external memory accesses. |
| $\overline{RD}$ | Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads. |
| $\overline{WR}$/$\overline{WRL}$ | Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}$/$\overline{WRL}$ is activated only during external memory writes. |

## PIN DESCRIPTIONS (Continued)

| Symbol | Name and Function |
|---|---|
| $\overline{BHE}/\overline{WRH}$ | Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects the bank of memory that is connected to the low byte of the data bus. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, $\overline{BHE}$ = 1), to the high byte only (A0 = 1, $\overline{BHE}$ = 0), or both bytes (A0 = 0, $\overline{BHE}$ = 0). If the $\overline{WRH}$ function is selected, the pin will go low if the bus cycle is writing to an odd memory location. $\overline{BHE}/\overline{WRH}$ is valid only during 16-bit external memory write cycles. |
| READY | Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait mode until the next positive transition in CLKOUT occurs with READY high. When the external memory is not being used, READY has no effect. Internal control of the number of wait states inserted into a bus cycle held not ready is available through configuration of CCR. |
| HSI | Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2, and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit. The HSI pins are also used as the SID in Slave Programming Mode on the EPROM device. |
| HSO | Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSO.3, HSO.4, and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit. |
| Port 0 | 8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins set the Programming Mode on the EPROM device. |
| Port 1 | 8-bit quasi-bidirectional I/O port. |
| Port 2 | 8-bit multi-functional port. All of its pins are shared with other functions in the 80C196KB. |
| Ports 3 and 4 | 8-bit bi-directional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups. Available as I/O only on the ROM and EPROM devices. |
| $\overline{HOLD}$ | Bus Hold input requesting control of the bus. Enabled by setting WSR.7. |
| $\overline{HLDA}$ | Bus Hold acknowledge output indicating release of the bus. Enabled by setting WSR.7. |
| $\overline{BREQ}$ | Bus Request output activated when the bus controller has a pending external memory cycle. Enabled by setting WSR.7. |
| TxD | The TxD pin is used for serial port transmission in Modes 1, 2, and 3. The TxD function is enabled by setting IOC1 5. In mode 0 the pin is used as the serial clock output. |
| RxD | Serial Port Receive pin used for serial port reception. The RxD function is enabled by setting SPCON.3. In mode 0 the pin functions as input or output data. |
| EXTINT | A rising edge on the EXTINT pin will generate an external interrupt. EXTINT is selected as the external interrupt source by setting IOC1.1 high. |
| T2CLK | The T2CLK pin is the Timer2 clock input or the serial port baud rate generator input. |
| T2RST | A rising edge on the T2RST pin will reset Timer2. The external reset function is enabled by setting IOCO.03 T2RST is enabled as the reset source by clearing IOCO.5. |
| PWM | Port 2.5 can be enabled as a PWM output by setting IOC1.O The duty cycle of the PWM is determined by the value loaded into the PWM-CONTROL register (17H). |
| T2UPDN | The T2UPDN pin controls the direction of Timer2 as an up or down counter. The Timer2 up/down function is enabled by setting IOC2.1. |
| T2CAP | A rising edge on P2.7 will capture the value of Timer2 in the T2CAPTURE register (location 0CH in Window 15). |

## NEW INSTRUCTIONS

The following five instructions have been added to the 8096BH instruction set for the 80C196KB.

PUSHA — PUSHes the PSW, IMASK, IMASK1, and WSR
(Used instead of PUSHF when new interrupts and registers are used.)

assembly language format: PUSHA
object code format: <11110100>
bytes: 1
states: on-chip stack: 12
off-chip stack: 18

POPA — POPs the PSW, IMASK, IMASK1, and WSR
(Used instead of POPF when new interrupts and registers are used.)

assembly language format: POPA
object code format: <11110101>
bytes: 1
states: on-chip stack: 12
off-chip stack:18

IDLPD — Sets the part into Idle or Powerdown Mode

assembly language format: IDLPD #key (key=1 for Idle, key=2 for Powerdown.)
object code format: <11110110> <key>
bytes: 2
states: legal key: 8
illegal key: 25

CMPL — Compare 2 long direct values

assembly language format:

```
                DST  SRC
CMPL            Lreg, Lreg
```

object code format: <11000101> <src Lreg> <dst Lreg>
bytes: 3
states: 7

BMOV — Block move using 2 auto-incrementing pointers and a counter

assembly language format:

```
                PTRS  CNTREG
BMOV            Lreg, wreg
```

object code format: <11000001> <wreg> <Lreg>
bytes: 3
states: internal/internal: 8 per transfer + 6
external/internal: 11 per transfer + 6
external/external: 14 per transfer + 6

## SFR OPERATION

All of the registers that were present on the 8096BH work the same way as they did, except that the baud rate value is different. The new registers shown in the memory map control new functions. The most important new register is the Window Select Register (WSR) which allows reading of the formerly write-only registers and vice-versa.

## USING THE ALTERNATE REGISTER WINDOW (WSR = 15)

I/O register expansion on the new CHMOS members of the MCS-96 family has been provided by making two register windows available. Switching between these windows is done using the Window Select Register (WSR). The PUSHA and POPA instructions can be used to push and pop the WSR and second interrupt mask when entering or leaving interrupts, so it is easy to change between windows.

On the 80C196KB only Window 0 and Window 15 are active. Window 0 is a true superset of the standard 8096BH SFR space, while Window 15 allows the read-only registers to be written and write-only registers to be read. The only major exception to this is the Timer2 register which is the Timer2 capture register in Window 15. The writeable register for Timer2 is in Window 0. There are also some minor changes and cautions. The descriptions of the registers which have different functions in Window 15 than in Window 0 are listed below:

| | |
|---|---|
| AD_COMMAND (02H) | — Read the last written command |
| AD_RESULT (02H, 03H) | — Write a value into the result register |
| HSI_MODE (03H) | — Read the value in HSI_MODE |
| HSI_TIME (04H,05H) | — Write to FIFO Holding register |
| HSO_TIME (04H,05H) | — Read the last value placed in the holding register |
| HSI_STATUS (06H) | — Write to status bits but not to HSI pin bits. (Pin bits are 1,3,5,7). |
| HSO_COMMAND (06H) | — Read the last value placed in the holding register |
| SBUF(RX) (07H) | — Write a value into the receive buffer |
| SBUF(TX) (07H) | — Read the last value written to the transmit buffer |
| WATCHDOG(0AH) | — Read the value in the upper byte of the WDT |
| TIMER1 (0AH,0BH) | — Write a value to Timer1 |
| TIMER2 (0CH,0DH) | — Read/Write the Timer2 capture register. Note that Timer2 read/write is done with WSR = 0. |
| IOC2 (0BH) | — Last written value is readable, except bit 7 (note 1) |
| BAUDRATE (0EH) | — No function, cannot be read |
| PORT0 (0EH) | — No function, no output drivers on the pins. Register reserved. |
| PORT1 | — IOPORT1 cannot be read or written in Window 15. Register reserved. |
| SP_STAT (11H) | — Set the status bits, TI and RI can be set, but it will not cause an interrupt |
| SP_CON (11H) | — Read the current control byte |
| IOS0 (15H) | — Writing to this register controls the HSO pins. Bits 6 and 7 are inactive for writes. |
| IOC0 (15H) | — Last written value is readable, except bit 1 (note 1) |
| IOS1 (16H) | — Writing to this register will set the status bits, but not cause interrupts. Bits 6 and 7 are not functional |
| IOC1 (16H) | — Last written value is readable |
| IOS2 (17H) | — Writing to this register will set the status bits, but not cause interrupts |

the duty cycle value written to PWM_CONTROL

PWM_CONTROL (17H) — Reac

**NOTE:**

1. (T2RST) are not latched and will read as a 1 (precharged bus).
1, IOC2.7 (CAM CLEAR) and IOC

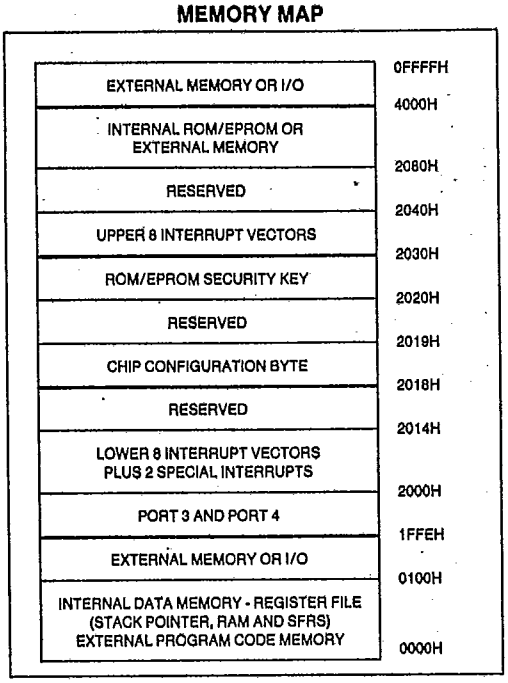
registers and vice-versa provides a lot of flexibility. One of the most useful
timers and HSO lines for initial conditions other than zero.

Being able to write to the read-only
advantages is the ability to set the

or testing or for future features. Do not write to these registers. Reads from
erminate values.

Reserved registers may be used fo
reserved registers will return indet

## MEMORY MAP




## 80C196KB INTERRUPTS

| Number | Source | Vector Location | Priority |
|---|---|---|---|
| INT15 | NMI | 203EH | 15 |
| INT14 | HSI FIFO Full | 203CH | 14 |
| INT13 | EXTINT Pin | 203AH | 13 |
| INT12 | TIMER2 Overflow | 2038H | 12 |
| INT11 | TIMER2 Capture | 2036H | 11 |
| INT10 | 4th Entry Into HSI FIFO | 2034H | 10 |
| INT09 | RI | 2032H | 9 |
| INT08 | TI | 2030H | 8 |
| SPECIAL | Unimplemented Opcode | 2012H | N/A |
| SPECIAL | Trap | 2010H | N/A |
| INT07 | EXTINT | 200EH | 7 |
| INT06 | Serial Port | 200CH | 6 |
| INT05 | Software Timer | 200AH | 5 |
| INT04 | HSI.0 Pin | 2008H | 4 |
| INT03 | High Speed Outputs | 2006H | 3 |
| INT02 | HSI Data Available | 2004H | 2 |
| INT01 | A/D Conversion Complete | 2002H | 1 |
| INT00 | Timer Overflow | 2000H | 0 |

4

| | WSR = 0 WHEN READ | WSR = 0 WHEN WRITTEN | WSR = 15 |
|---|---|---|---|
| 19H | STACK POINTER | STACK POINTER | |
| 18H | | | |
| 17H | *IOS2 | PWM_CONTROL | |
| 16H | IOS1 | IOC1 | |
| 15H | IOS0 | IOC0 | |
| 14H | *WSR | *WSR | |
| 13H | *INT_MASK 1 | *INT_MASK 1 | |
| 12H | *INT_PEND 1 | *INT_PEND 1 | |
| 11H | *SP_STAT | *SP_CON | |
| 10H | PORT2 | PORT2 | |
| 0FH | PORT1 | PORT1 | RESERVED (1) |
| 0EH | PORT0 | BAUD RATE | RESERVED (1) |
| 0DH | TIMER2 (HI) | TIMER2 (HI) | RESERVED (1) |
| 0CH | TIMER2 (LO) | TIMER2 (LO) | *T2 CAPTURE (HI) |
| 0BH | TIMER1 (HI) | *IOC2 | *T2 CAPTURE (LO) |
| 0AH | TIMER1 (LO) | WATCHDOG | |
| 09H | INT_PENDING | INT_PENDING | |
| 08H | INT_MASK | INT_MASK | |
| 07H | SBUF(RX) | SBUF(TX) | |
| 06H | HSI_STATUS | HSO_COMMAND | |
| 05H | HSI_TIME (HI) | HSO_TIME (HI) | |
| 04H | HSI_TIME (LO) | HSO_TIME (LO) | |
| 03H | AD_RESULT (HI) | HSI_MODE | |
| 02H | AD_RESULT (LO) | AD_COMMAND | |
| 01H | ZERO REG (HI) | ZERO REG (HI) | |
| 00H | ZERO REG (LO) | ZERO REG (LO) | |

OTHER SFRS IN WSR 15 BECOME READABLE IF THEY WERE WRITABLE IN WSR = 0 AND WRITABLE IF THEY WERE READABLE IN WSR = 0

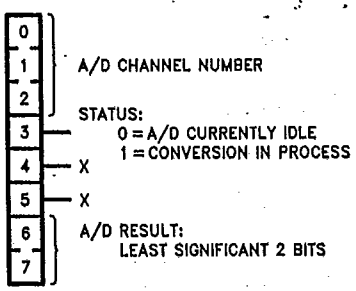
*NEW OR CHANGED REGISTER FUNCTION FROM 8096BH

**NOTE:**
1. Reserved registers should not be written.

## SFR BIT SUMMARY

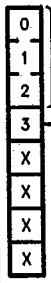
T-49-19-59

### AD—Result (LO) (02H)




270918-7

### AD_Command (02H)



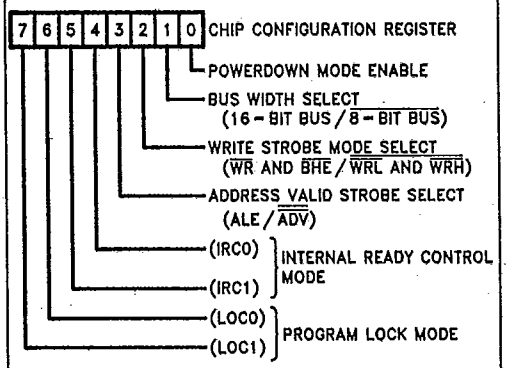

CHANNEL # SELECTS WHICH OF THE 8 ANALOG INPUT CHANNELS IS TO BE CONVERTED TO DIGITAL FORM.

GO INDICATES WHEN THE CONVERSION IS TO BE INITIATED (GO = 1 MEANS START NOW, GO = 0 MEANS THE CONVERSION IS TO BE INITIATED BY THE HSO UNIT AT A SPECIFIED TIME).

SET UPPER FOUR BITS TO ZERO

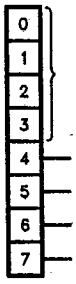
270918-8

### Chip Configuration (2018H)




270918-9

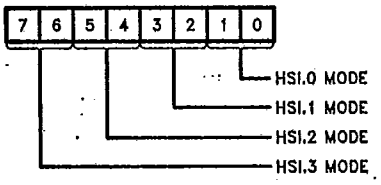
### WSR (14H)




Ø = SFR's FUNCTION LIKE SUPERSET OF 8096BH
14(1110B) = PPW REGISTER
15(1111B) = EXCHANGE READ/WRITE REGISTERS
OTHER = UNDEFINED, DO NOT USE

270918-10

### HSI_Mode (03H)

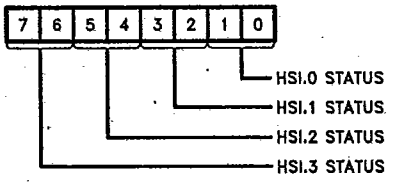



WHERE EACH 2-BIT MODE CONTROL FIELD DEFINES ONE OF 4 POSSIBLE MODES:

00 8 POSITIVE TRANSITIONS
01 EACH POSITIVE TRANSITION
10 EACH NEGATIVE TRANSITION
11 EVERY TRANSITION (POSITIVE AND NEGATIVE)

270918-11

### HSI_Status (06H)

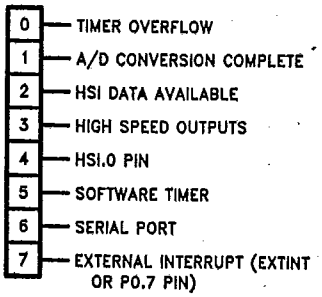



WHERE FOR EACH 2-BIT STATUS FIELD THE LOWER BIT INDICATES WHETHER OR NOT AN EVENT HAS OCCURED ON THIS PIN AND THE UPPER BIT INDICATES THE CURRENT STATUS OF THE PIN.

270918-12

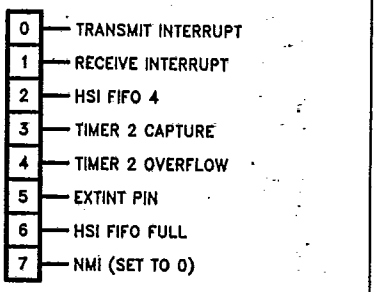
T-49-19-16 T-49-19-59

**INT_PEND/INT_MASK (09H/08H)**



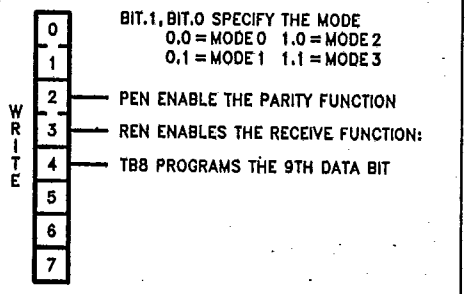

270918-13

**INT_PEND1/INT_MASK1 (12H/13H)**



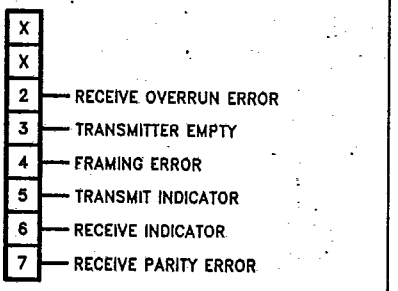

270918-14

**SP_CON (11H)**



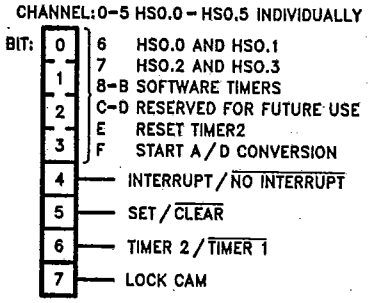

270918-15

**SP_STAT (11H)**




270918-16

**HSO Command (06H)**




270918-17

**IOS0 (15H)**

| | |
|---|---|
| 0 | HSO.0 CURRENT STATE |
| 1 | HSO.1 CURRENT STATE |
| 2 | HSO.2 CURRENT STATE |
| 3 | HSO.3 CURRENT STATE |
| 4 | HSO.4 CURRENT STATE |
| 5 | HSO.5 CURRENT STATE |
| 6 | CAM OR HOLDING REGISTER IS FULL |
| 7 | HSO HOLDING REGISTER IS FULL |

270918-18

**IOC0 (15H)**

| | |
|---|---|
| 0 | HSI.0 INPUT ENABLE / $\overline{\text{DISABLE}}$ |
| 1 | TIMER 2 RESET EACH WRITE |
| 2 | HSI.1 INPUT ENABLE / $\overline{\text{DISABLE}}$ |
| 3 | TIMER 2 EXTERNAL RESET ENABLE / $\overline{\text{DISABLE}}$ |
| 4 | HSI.2 INPUT ENABLE / $\overline{\text{DISABLE}}$ |
| 5 | TIMER 2 RESET SOURCE HSI.0 / $\overline{\text{T2RST}}$ |
| 6 | HSI.3 INPUT ENABLE / $\overline{\text{DISABLE}}$ |
| 7 | TIMER 2 CLOCK SOURCE HSI.1 / $\overline{\text{T2CLK}}$ |

270918-19

**IOS1 (16H)**

| | |
|---|---|
| 0 | SOFTWARE TIMER 0 EXPIRED |
| 1 | SOFTWARE TIMER 1 EXPIRED |
| 2 | SOFTWARE TIMER 2 EXPIRED |
| 3 | SOFTWARE TIMER 3 EXPIRED |
| 4 | TIMER 2 HAS OVERFLOW |
| 5 | TIMER 1 HAS OVERFLOW |
| 6 | HSI FIFO IS FULL |
| 7 | HSI HOLDING REGISTER DATA AVAILABLE |

270918-20

**IOC1 (16H)**

| | |
|---|---|
| 0 | SELECT PWM / $\overline{\text{SELECT P2.5}}$ |
| 1 | EXTERNAL INTERRUPT ACH7 / $\overline{\text{EXTINT}}$ |
| 2 | TIMER 1 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$ |
| 3 | TIMER 2 OVERFLOW INTERRUPT ENABLE / $\overline{\text{DISABLE}}$ |
| 4 | HSO.4 OUTPUT ENABLE / $\overline{\text{DISABLE}}$ |
| 5 | SELECT TXD / $\overline{\text{SELECT P2.0}}$ |
| 6 | HSO.5 OUTPUT ENABLE / $\overline{\text{DISABLE}}$ |
| 7 | HSI INTERRUPT FIFO FULL / $\overline{\text{HOLDING REGISTER LOADED}}$ |

270918-21

**IOS2 (17H)**

INDICATES WHICH HSO EVENT OCCURED

| | |
|---|---|
| 0 | HSO.0 |
| 1 | HSO.1 |
| 2 | HSO.2 |
| 3 | HSO.3 |
| 4 | HSO.4 |
| 5 | HSO.5 |
| 6 | T2RESET |
| 7 | START A/D |

270918-22

**IOC2 (0BH)**

| | |
|---|---|
| 0 | ENABLE T2 AS INCREMENT ONLY |
| 1 | ENABLE T2 AS UP/DOWN COUNTER |
| 2 | ENABLE ÷2 PRESCALER ON PWM |
| 3 | X (SET TO 0) |
| 4 | A/D CLOCK PRESCALER DISABLE |
| 5 | T2 ALTERNATE INTERRUPT @ 8000H |
| 6 | ENABLE LOCKED CAM ENTRIES |
| 7 | CLEAR ENTIRE CAM |

270918-23

T-49-19-16 T-49-19-59

## ELECTRICAL CHARACTERISTICS

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

### Absolute Maximum Ratings*

Ambient Temperature
Under Bias.....0°C to +70°C
Storage Temperature .....−65°C to +150°C
Voltage On Any Pin to $V_{SS}$.....−0.5V to +7.0V
Power Dissipation.....1.5W

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

### Operating Conditions

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_A$ | Ambient Temperature Under Bias | 0 | +70 | °C |
| $V_{CC}$ | Digital Supply Voltage | 4.50 | 5.50 | V |
| $V_{REF}$ | Analog Supply Voltage | 4.50 | 5.50 | V |
| $f_{OSC}$ | Oscillator Frequency | 3.5 | 12 | MHz |

**NOTE:**
ANGND and $V_{SS}$ should be nominally at the same potential.

### D.C. Characteristics (Over Specified Operating Conditions)

| Symbol | Description | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage (Note 1) | 0.2 $V_{CC}$ + 0.9 | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage on XTAL 1 | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{IH2}$ | Input High Voltage on RESET | 2.6 | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage | | 0.3<br>0.45<br>1.5 | V<br>V<br>V | $I_{OL}$ = 200 µA<br>$I_{OL}$ = 3.2 mA<br>$I_{OL}$ = 7 mA |
| $V_{OH}$ | Output High Voltage (Standard Outputs) | $V_{CC}$ − 0.3<br>$V_{CC}$ − 0.7<br>$V_{CC}$ − 1.5 | | V<br>V<br>V | $I_{OH}$ = −200 µA<br>$I_{OH}$ = −3.2 mA<br>$I_{OH}$ = −7 mA |
| $V_{OH1}$ | Output High Voltage (Quasi-bidirectional Outputs) | $V_{CC}$ − 0.3<br>$V_{CC}$ − 0.7<br>$V_{CC}$ − 1.5 | | V<br>V<br>V | $I_{OH}$ = −10 µA<br>$I_{OH}$ = −30 µA<br>$I_{OH}$ = −60 µA |
| $I_{LI}$ | Input Leakage Current (Std. Inputs) | | ±10 | µA | 0 < $V_{IN}$ < $V_{CC}$ − 0.3V |
| $I_{LI1}$ | Input Leakage Current (Port 0) | | +3 | µA | 0 < $V_{IN}$ < $V_{REF}$ |
| $I_{TL}$ | 1 to 0 Transition Current (QBD Pins) | | −650 | µA | $V_{IN}$ = 2.0V |
| $I_{IL}$ | Logical 0 Input Current (QBD Pins) | | −50 | µA | $V_{IN}$ = 0.45V |
| $I_{IL1}$ | Logical 0 Input Current in Reset (Note 2) (ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, INST, P2.0) | | −1.2 | mA | $V_{IN}$ = 0.45 V |
| Hyst | Hysteresis on RESET Pin | 300 | | mV | (Note 3) |

**NOTES:**
1. All pins except RESET and XTAL1.
2. Holding these pins below $V_{IH}$ in Reset may cause the part to enter test modes.
3. Not guaranteed for the 87C196KB.

## D.C. Characteristics (Continued)

| Symbol | Description | Min | Typ(7) | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Active Mode Current in Reset | | 40 | 55 | mA | XTAL1 = 12 MHz<br>$V_{CC} = V_{PP} = V_{REF} = 5.5V$ |
| $I_{REF}$ | A/D Converter Reference Current | | 2 | 5 | mA | |
| $I_{IDLE}$ | Idle Mode Current | | 10 | 22 | mA | |
| $I_{CC1}$ | Active Mode Current | | 15 | 22 | mA | XTAL1 = 3.5 MHz |
| $I_{PD}$ | Powerdown Mode Current | | 5 | 50 | µA | $V_{CC} = V_{PP} = V_{REF} = 5.5V$ |
| $R_{RST}$ | Reset Pullup Resistor | 6K | | 50K | Ω | |
| $C_S$ | Pin Capacitance (Any Pin to $V_{SS}$) | | | 10 | pF | $f_{TEST}$ = 1.0 MHz |

**NOTES:**
(Notes apply to all specifications)
1. QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
2. Standard Outputs include AD0–15, $\overline{RD}$, $\overline{WR}$, ALE, $\overline{BHE}$, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0, and RXD (in serial mode 0). The $V_{OH}$ specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
3. Standard Inputs include HSI pins, CDE, $\overline{EA}$, READY, BUSWIDTH, NMI, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3, and T2RST/P2.4.
4. Maximum current per pin must be externally limited to the following values if $V_{OL}$ is held above 0.45V or $V_{OH}$ is held below $V_{CC}$ − 0.7V:
   $I_{OL}$ on Output pins: 10 mA
   $I_{OH}$ on quasi-bidirectional pins: self limiting
   $I_{OH}$ on Standard Output pins: 10 mA
5. Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
6. During normal (non-transient) conditions the following total current limits apply:

| | | |
|---|---|---|
| Port 1, P2.6 | $I_{OL}$: 29 mA | $I_{OH}$ is self limiting |
| HSO, P2.0, RXD, $\overline{RESET}$ | $I_{OL}$: 29 mA | $I_{OH}$: 26 mA |
| P2.5, P2.7, $\overline{WR}$, $\overline{BHE}$ | $I_{OL}$: 13 mA | $I_{OH}$: 11 mA |
| AD0–AD15 | $I_{OL}$: 52 mA | $I_{OH}$: 52 mA |
| $\overline{RD}$, ALE, INST–CLKOUT | $I_{OL}$: 13 mA | $I_{OH}$: 13 mA |

7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.

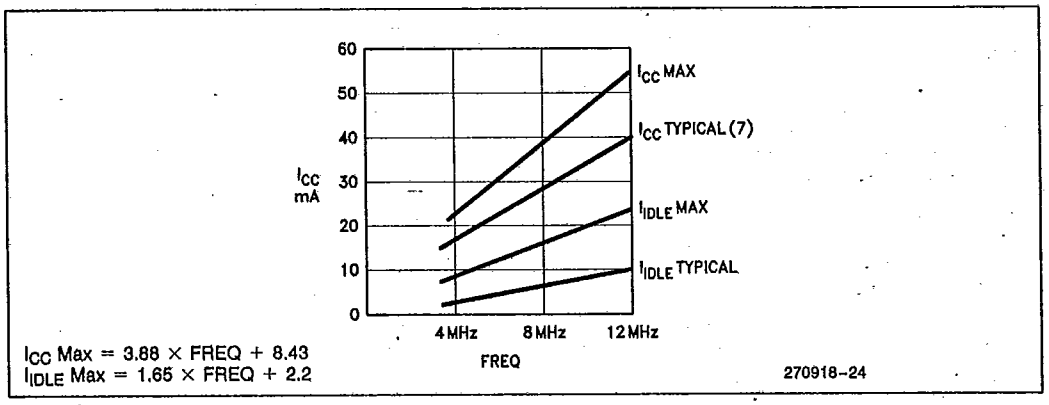



**Figure 7. $I_{CC}$ and $I_{IDLE}$ vs Frequency**

## A.C. Characteristics

For use over specified operating conditions

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, $f_{OSC}$ = 12 MHz

**The system must meet these specifications to work with the 80C196KB: (Note 1)**

| Symbol | Description | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $T_{AVYV}$ | Address Valid to Ready Setup<br>87C196KB10/83C196KB10<br>87C196KB12/83C196KB12/80C196KB | | <br>$2T_{OSC} - 90$<br>$2T_{OSC} - 85$ | <br>ns<br>ns | |
| $T_{LLYV}$ | ALE Low to READY Setup<br>80C196KB<br>87C196KB10/83C196KB10<br>87C196KB12/83C196KB12 | | <br>$T_{OSC} - 65$<br>$T_{OSC} - 80$<br>$T_{OSC} - 72$ | <br>ns<br>ns<br>ns | |
| $T_{YLYH}$ | Non READY Time | No upper limit | | ns | |
| $T_{CLYX}$ | READY Hold after CLKOUT Low | 0 | $T_{OSC} - 30$ | ns | (Note 2) |
| $T_{LLYX}$ | READY Hold after ALE Low | $T_{OSC} - 15$ | $2T_{OSC} - 40$ | ns | (Note 2) |
| $T_{AVGV}$ | Address Valid to Buswidth Setup | | $2T_{OSC} - 85$ | ns | |
| $T_{LLGV}$ | ALE Low to Buswidth Setup<br>80C196KB<br>87C196KB/83C196KB | | <br>$T_{OSC} - 60$<br>$T_{OSC} - 70$ | <br>ns<br>ns | |
| $T_{CLGX}$ | Buswidth Hold after CLKOUT Low | 0 | | ns | |
| $T_{AVDV}$ | Address Valid to Input Data Valid<br>80C196KB<br>87C196KB10/83C196KB10<br>87C196KB12/83C196KB12 | | <br>$3T_{OSC} - 60$<br>$3T_{OSC} - 70$<br>$3T_{OSC} - 67$ | <br>ns<br>ns<br>ns | (Note 3) |
| $T_{RLDV}$ | $\overline{RD}$ Active to Input Data Valid<br>87C196KB10/83C196KB10<br>87C196KB12/83C196KB12/80C196KB | | <br>$T_{OSC} - 30$<br>$T_{OSC} - 23$ | <br>ns<br>ns | (Note 3) |
| $T_{CLDV}$ | CLKOUT Low to Input Data Valid | | $T_{OSC} - 50$ | ns | |
| $T_{RHDZ}$ | End of $\overline{RD}$ to Input Data Float | | $T_{OSC} - 20$ | ns | |
| $T_{RXDX}$ | Data Hold after $\overline{RD}$ Inactive | 0 | | ns | |

**NOTES:**
1. Customers whose applications require an 83C196KB to meet the 80C196KB specifications listed above should contact an Intel Field Sales Representative.
2. If max is exceeded, additional wait states will occur.
3. When using wait states, add $2T_{OSC} \times n$, where n = number of wait states.

## A.C. Characteristics

For use over specified operating conditions

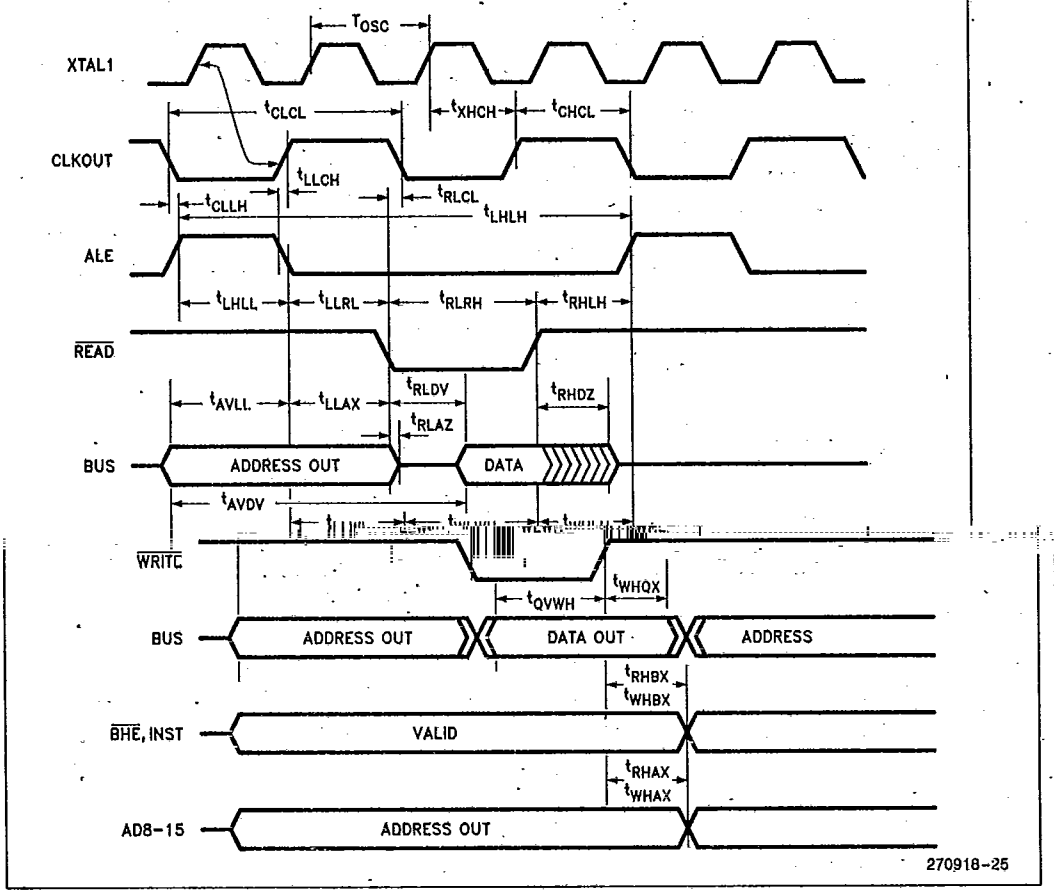
Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, $f_{OSC}$ = 12 MHz

**The 80C196KB will meet these specifications: (Note 1)**

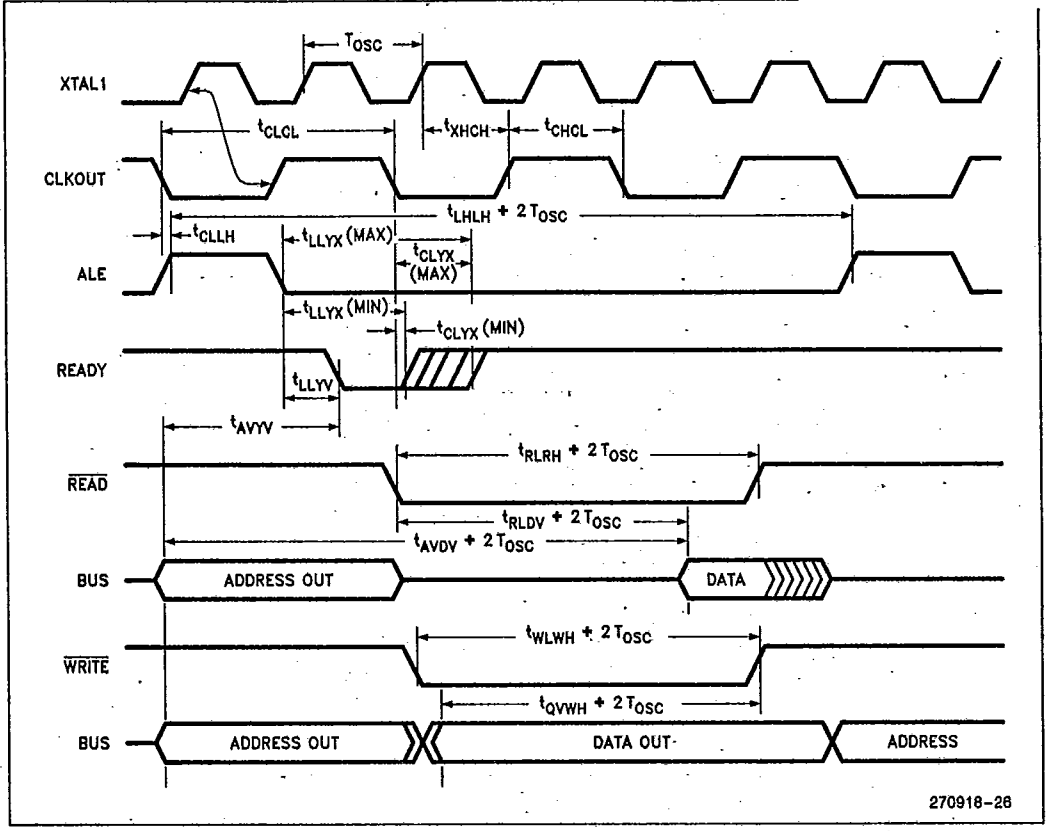
| Symbol | Description | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $F_{XTAL}$ | Frequency on XTAL1<br>87C196KB10/83C196KB10<br>87C196KB12/83C196KB12/80C196KB | 3.5<br>3.5 | 10<br>12 | MHz<br>MHz | (Note 2)<br>(Note 2) |
| $T_{OSC}$ | 1/$F_{XTAL}$<br>87C196KB10/83C196KB10<br>87C196KB12/83C196KB12/80C196KB | 100<br>83 | 286<br>286 | ns<br>ns | |
| $T_{XHCH}$ | XTAL1 High to CLKOUT High or Low | 40 | 110 | ns | (Note 3) |
| $T_{CLCL}$ | CLKOUT Cycle Time | $2T_{OSC}$ | | ns | |
| $T_{CHCL}$ | CLKOUT High Period | $T_{OSC}$ − 10 | $T_{OSC}$ + 10 | ns | |
| $T_{CLLH}$ | CLKOUT Falling Edge to ALE Rising | −5 | 15 | ns | |
| $T_{LLCH}$ | ALE Falling Edge to CLKOUT Rising | −15 | 15 | ns | |
| $T_{LHLH}$ | ALE Cycle Time | $4T_{OSC}$ | | ns | (Note 5) |
| $T_{LHLL}$ | ALE High Period | $T_{OSC}$ − 10 | $T_{OSC}$ + 10 | ns | |
| $T_{AVLL}$ | Address Setup to ALE Falling Edge | $T_{OSC}$ − 20 | | | |
| $T_{LLAX}$ | Address Hold after ALE Falling Edge | $T_{OSC}$ − 40 | | ns | |
| $T_{LLRL}$ | ALE Falling Edge to $\overline{RD}$ Falling Edge<br>80C196KB<br>87C196KB/83C196KB | <br>$T_{OSC}$ − 30<br>$T_{OSC}$ − 40 | | <br>ns<br>ns | |
| $T_{RLCL}$ | $\overline{RD}$ Low to CLKOUT Falling Edge | 5 | 30 | ns | |
| $T_{RLRH}$ | $\overline{RD}$ Low Period | $T_{OSC}$ − 5 | $T_{OSC}$ + 25 | ns | (Note 5) |
| $T_{RHLH}$ | $\overline{RD}$ Rising Edge to ALE Rising Edge | $T_{OSC}$ | $T_{OSC}$ + 25 | ns | (Note 4) |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float | | 10 | ns | |
| $T_{LLWL}$ | ALE Falling Edge to $\overline{WR}$ Falling Edge | $T_{OSC}$ − 10 | | ns | |
| $T_{CLWL}$ | CLKOUT Low to $\overline{WR}$ Falling Edge | 0 | 25 | ns | |
| $T_{QVWH}$ | Data Stable to $\overline{WR}$ Rising Edge<br>87C196KB10/83C196KB10<br>87C196KB12/83C196KB12/80C196KB | <br>$T_{OSC}$ − 30<br>$T_{OSC}$ − 23 | | <br>ns<br>ns | (Note 5) |
| $T_{CHWH}$ | CLKOUT High to $\overline{WR}$ Rising Edge | −10 | 10 | ns | |
| $T_{WLWH}$ | $\overline{WR}$ Low Period | $T_{OSC}$ − 30 | $T_{OSC}$ + 5 | ns | (Note 5) |
| $T_{WHQX}$ | Data Hold after $\overline{WR}$ Rising Edge | $T_{OSC}$ − 10 | | ns | |
| $T_{WHLH}$ | $\overline{WR}$ Rising Edge to ALE Rising Edge | $T_{OSC}$ − 10 | $T_{OSC}$ + 15 | ns | (Note 4) |
| $T_{WHBX}$ | $\overline{BHE}$, INST Hold after $\overline{WR}$ Rising Edge | $T_{OSC}$ − 10 | | ns | |
| $T_{RHBX}$ | $\overline{BHE}$, INST Hold after $\overline{RD}$ Rising Edge | $T_{OSC}$ − 10 | | ns | |
| $T_{WHAX}$ | AD8–15 Hold after $\overline{WR}$ Rising Edge | $T_{OSC}$ − 50 | | ns | |
| $T_{RHAX}$ | AD8–15 Hold after $\overline{RD}$ Rising Edge | $T_{OSC}$ − 25 | | ns | |

**NOTES:**
$T_{OSC}$ = 83.3 ns at 12 MHz; $T_{OSC}$ = 100 ns at 10 MHz.
1. Customers whose applications require an 83C196KB to meet the 80C196KB specifications listed above should contact an Intel Field Sales Representative.
2. Testing performed at 3.5 MHz. However, the part is static by design and will typically operate below 1 Hz.
3. Typical specification, not guaranteed.
4. Assuming back-to-back bus cycles.
5. When using wait states, add $2T_{OSC} \times n$, where n = number of wait states.

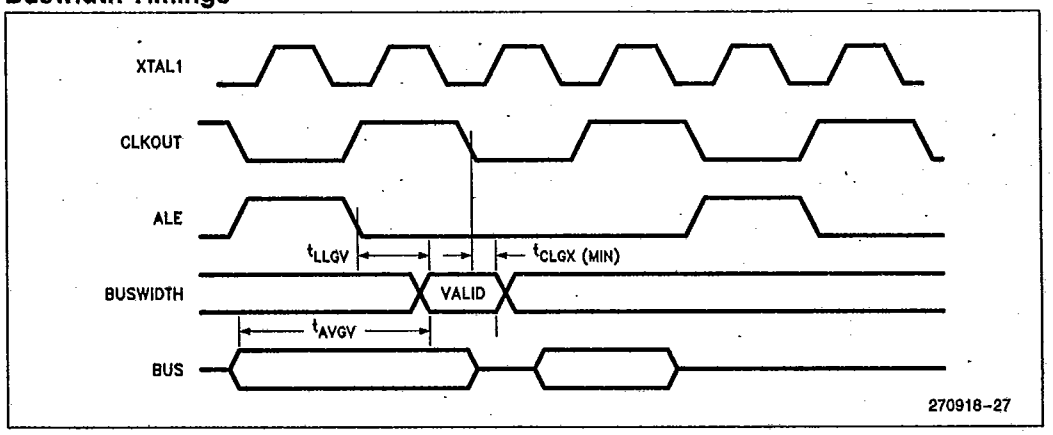
## System Bus Timings



## READY Timings (One Waitstate)



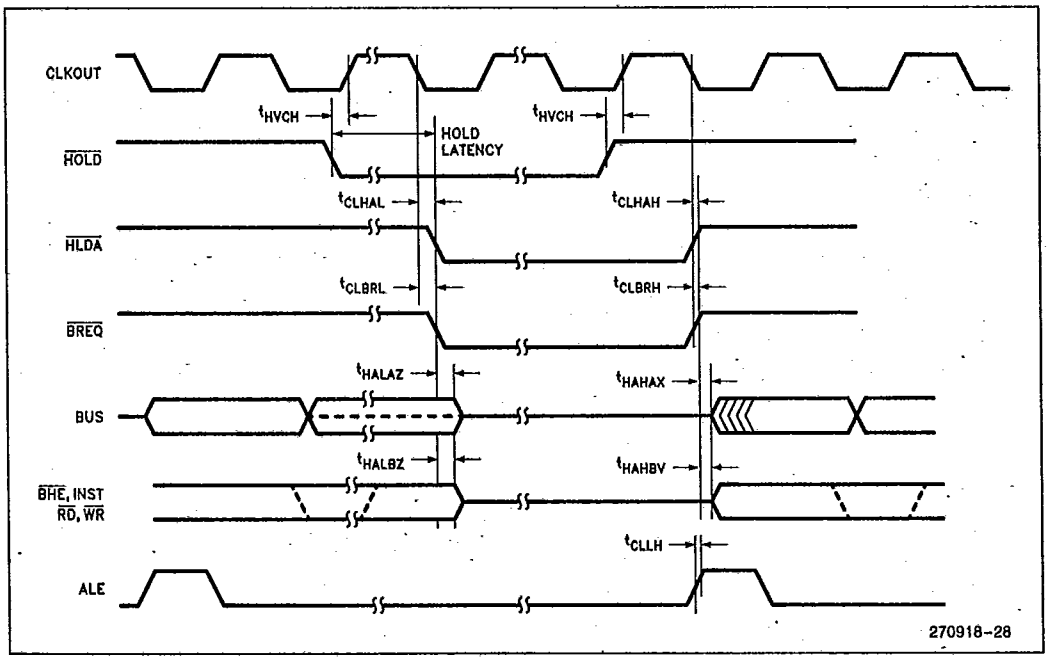

## Buswidth Timings



## HOLD/HLDA TIMINGS

| Symbol | Description | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $T_{HVCH}$ | HOLD Setup<br>80C196KB<br>87C196KB/83C196KB | <br>75<br>85 | | ns | 1 |
| $T_{CLHAL}$ | CLKOUT Low to HLDA Low | −15 | 15 | ns | |
| $T_{CLBRL}$ | CLKOUT Low to BREQ Low | −15 | 15 | ns | |
| $T_{HALAZ}$ | HLDA Low to Address Float<br>80C196KB<br>87C196KB/83C196KB | | <br>15<br>20 | ns | |
| $T_{HALBZ}$ | HLDA Low to BHE, INST, RD, WR Float | | | ns | |
| $T_{CLHAH}$ | CLKOUT Low to HLDA High | −15 | 15 | ns | |
| $T_{CLBRH}$ | CLKOUT Low to BREQ High | −15 | 15 | ns | |
| $T_{HAHAX}$ | HLDA High to Address No Longer Float | −5 | | ns | |
| $T_{HAHBV}$ | HLDA High to BHE, INST, RD, WR Valid | −20 | | ns | |
| $T_{CLLH}$ | CLKOUT Low to ALE High | −5 | 15 | ns | |

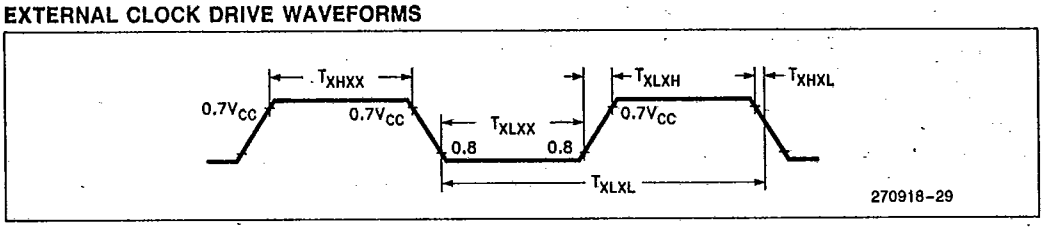
**NOTE:**
1. To guarantee recognition at next clock.



## EXTERNAL CLOCK DRIVE

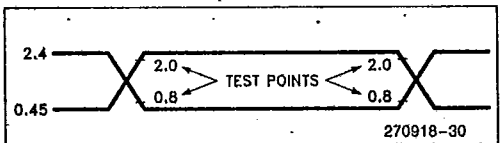
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $1/T_{XLXL}$ | Oscillator Frequency | | | |
| | 80C196KB10 | 3.5 | 10.0 | MHz |
| | 80C196KB12 | 3.5 | 12.0 | MHz |
| $T_{XLXL}$ | Oscillator Frequency | | | |
| | 80C196KB10 | 100 | 286 | ns |
| | 80C196KB12 | 83 | 286 | ns |
| $T_{XHXX}$ | High Time | 32 | | ns |
| $T_{XLXX}$ | Low Time | 32 | | ns |
| $T_{XLXH}$ | Rise Time | | 10 | ns |
| $T_{XHXL}$ | Fall Time | | 10 | ns |

### EXTERNAL CLOCK DRIVE WAVEFORMS



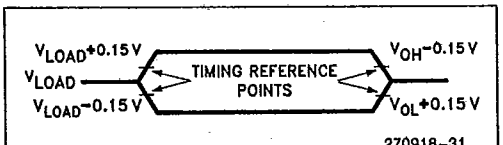

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts-up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the $V_{IL}$ and $V_{IH}$ specifications the capacitance will not exceed 20 pF.

### A.C. TESTING INPUT, OUTPUT WAVEFORM




A.C. Testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

### FLOAT WAVEFORM




For Timing Purposes a Port Pin is no Longer Floating when a 100 mV change from Load Voltage Occurs and Begins to Float when a 100 mV change from the Loaded $V_{OH}/V_{OL}$ Level occurs $I_{OL}/I_{OH} = \pm 15$ mA.

### EXPLANATION OF AC SYMBOLS

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

**Conditions:**

H - High
L - Low
V - Valid
X - No Longer Valid
Z - Floating

**Signals:**

A - Address
B - $\overline{BHE}$
BR - $\overline{BREQ}$
C - CLKOUT
D - DATA IN
G - Buswidth
H - $\overline{HOLD}$
HA - $\overline{HLDA}$
L - ALE/$\overline{ADV}$
Q - DATA OUT
R - $\overline{RD}$
W - $\overline{WR}$/$\overline{WRH}$/$\overline{WRL}$
X - XTAL1
Y - READY

## EPROM SPECIFICATIONS

### A.C. EPROM Programming Characteristics

Operating Conditions: Load Capacitance = 150 pF, $T_A$ = +25°C ±5°C, $V_{CC}$, $V_{REF}$ = 5V, $V_{SS}$, ANGND = 0V, $V_{PP}$ = 12.75V ± 0.25V, EA = 12.75V ± 0.25

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SHLL}$ | Reset High to First $\overline{PALE}$ Low | 1100 | | Tosc |
| $T_{LLLH}$ | $\overline{PALE}$ Pulse Width | 40 | | Tosc |
| $T_{AVLL}$ | Address Setup Time | 0 | | Tosc |
| $T_{LLAX}$ | Address Hold Time | 50 | | Tosc |
| $T_{LLVL}$ | $\overline{PALE}$ Low to PVER Low | | 60 | Tosc |
| $T_{PLDV}$ | $\overline{PROG}$ Low to Word Dump Valid | | 50 | Tosc |
| $T_{PHDX}$ | Word Dump Data Hold | | 50 | Tosc |
| $T_{DVPL}$ | Data Setup Time | 0 | | Tosc |
| $T_{PLDX}$ | Data Hold Time | 50 | | Tosc |
| $T_{PLPH}$ | $\overline{PROG}$ Pulse Width | 40 | | Tosc |
| $T_{PHLL}$ | $\overline{PROG}$ High to Next $\overline{PALE}$ Low | 120 | | Tosc |
| $T_{LHPL}$ | $\overline{PALE}$ High to $\overline{PROG}$ Low | 220 | | Tosc |
| $T_{PHPL}$ | $\overline{PROG}$ High to Next $\overline{PROG}$ Low | 120 | | Tosc |
| $T_{PHIL}$ | $\overline{PROG}$ High to $\overline{AINC}$ Low | 0 | | Tosc |
| $T_{ILIH}$ | $\overline{AINC}$ Pulse Width | 40 | | Tosc |
| $T_{ILVH}$ | PVER Hold after $\overline{AINC}$ Low | 50 | | Tosc |
| $T_{ILPL}$ | $\overline{AINC}$ Low to $\overline{PROG}$ Low | 170 | | Tosc |
| $T_{PHVL}$ | $\overline{PROG}$ High to PVER Low | | 90 | Tosc |

**NOTE:**
1. Run Time Programming is done with Fosc = 6.0 MHz to 12.0 MHz, $V_{REF}$ = 5V ± 0.65V. $T_A$ = +25°C to ±5°C and $V_{PP}$ = 12.75V. For run-time programming over a full operating range, contact the factory.

### D.C. EPROM Programming Characteristics

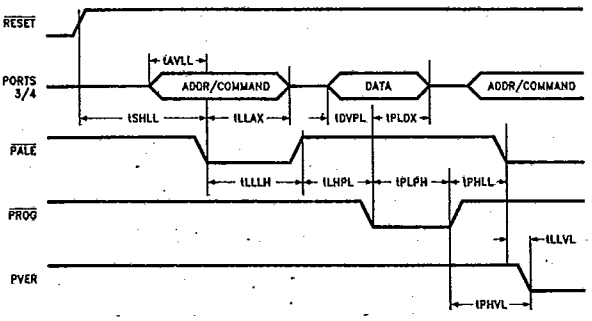
| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $I_{PP}$ | $V_{PP}$ Supply Current (When Programming) | | 100 | mA |

**NOTE:**
$V_{PP}$ must be within 1V of $V_{CC}$ while $V_{CC}$ < 4.5V. $V_{PP}$ must not have a low impedance path to ground or $V_{SS}$ while $V_{CC}$ > 4.5V.

## EPROM PROGRAMMING WAVEFORMS

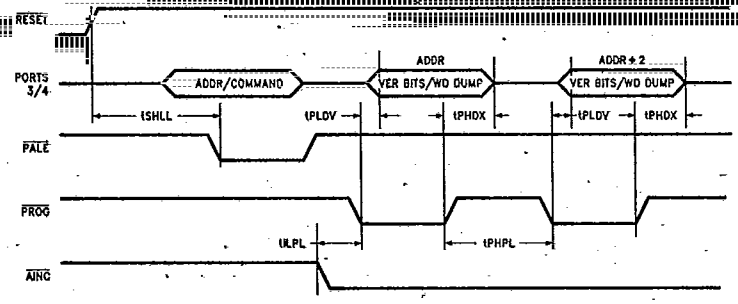
T-49-19-59

### SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE



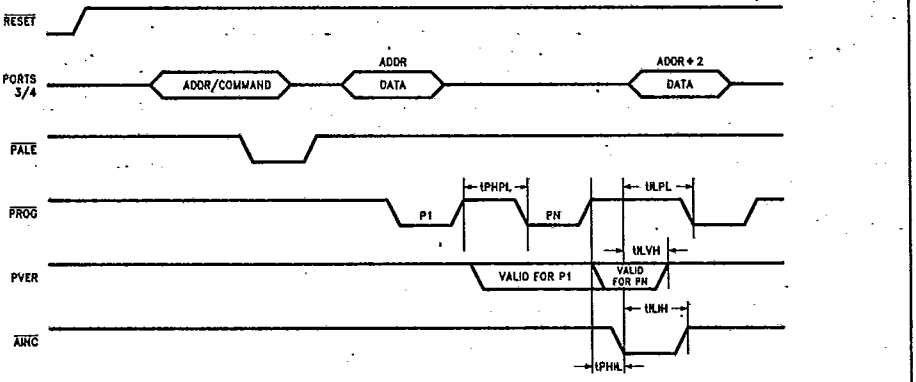

270918-32

### SLAVE PROGRAM MODE IN WORD DUMP OR DATA VERIFY MODE WITH AUTO INCREMENT




270918-33

### SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM MODE WITH REPEATED PROG PULSE AND AUTO INCREMENT




270918-34

## A.C. CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE

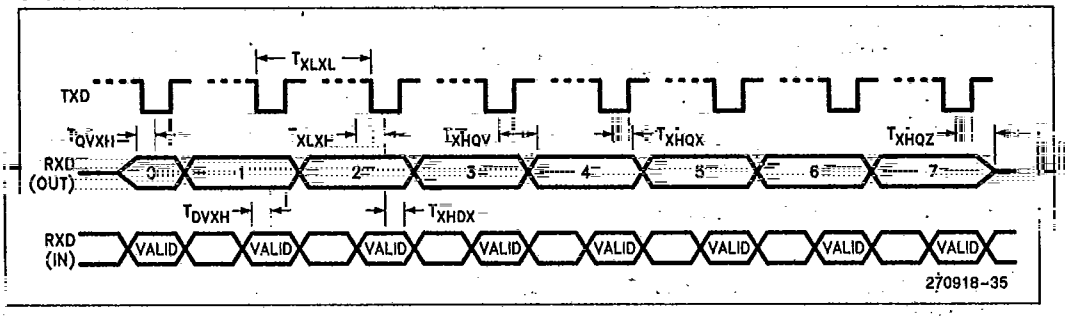
T-49-19-16 T-49-19-59

### SERIAL PORT TIMING—SHIFT REGISTER MODE

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{XLXL}$ | Serial Port Clock Period (BRR ≥ 8002H) | 6 $T_{OSC}$ | | ns |
| $T_{XLXH}$ | Serial Port Clock Falling Edge to Rising Edge (BRR ≥ 8002H) | 4 $T_{OSC}$ ±50 | | ns |
| $T_{XLXL}$ | Serial Port Clock Period (BRR = 8001H) | 4 $T_{OSC}$ | | ns |
| $T_{XLXH}$ | Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H) | 2 $T_{OSC}$ ±50 | | ns |
| $T_{QVXH}$ | Output Data Setup to Clock Rising Edge | 2 $T_{OSC}$ −50 | | ns |
| $T_{XHQX}$ | Output Data Hold after Clock Rising Edge | 2 $T_{OSC}$ −50 | | ns |
| $T_{XHQV}$ | Next Output Data Valid after Clock Rising Edge | | 2 $T_{OSC}$ +50 | ns |
| $T_{DVXH}$ | Input Data Setup to Clock Rising Edge | $T_{OSC}$ +50 | | ns |
| $T_{XHDX}$ | Input Data Hold after Clock Rising Edge | 0 | | ns |
| $T_{XHQZ}$ | Last Clock Rising to Output Float | | 1 $T_{OSC}$ | ns |

## WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE

### SERIAL PORT WAVEFORM—SHIFT REGISTER MODE



## A TO D CHARACTERISTICS

There are two modes of A/D operation: with or without clock prescaler. The speed of the A/D converter can be adjusted by setting a clock prescaler on or off. At high frequencies more time is needed for the comparator to settle. The maximum frequency with the clock prescaler disabled is 8 MHz. The conversion times with the prescaler turned on or off is shown in the table below.

The converter is ratiometric, so the absolute accuracy is directly dependent on the accuracy and stability of $V_{REF}$. $V_{REF}$ must be close to $V_{CC}$ since it supplies both the resistor ladder and the digital section of the converter.

| Clock Prescaler On IOC2.4 = 0 | Clock Prescaler Off IOC2.4 = 1 |
|---|---|
| 158 States<br>26.33 µs @ 12 MHz | 91 States<br>22.75 µs @ 8 MHz |

## A/D CONVERTER SPECIFICATIONS

The specifications given below assume adherence to the Operating Conditions section of this data sheet. Testing is performed with $V_{REF}$ = 5.12V.

| Parameter | Typical(1) | Minimum | Maximum | Units* | Notes |
|---|---|---|---|---|---|
| Resolution | | 512<br>9 | 1024<br>10 | Levels<br>Bits | |
| Absolute Error | | 0 | ±4 | LSBs | |
| Full Scale Error | 0.25 ±0.50 | | | LSBs | |
| Zero Offset Error | −0.25 ±0.50 | | | LSBs | |
| Non-Linearity Error | 1.5 ±2.5 | 0 | ±4 | LSBs | |
| Differential Non-Linearity Error | | >−1 | +2 | LSBs | |
| Channel-to-Channel Matching | ±0.1 | 0 | ±1 | LSBs | |
| Repeatability | ±0.25 | | | LSBs | |
| Temperature Coefficients:<br>Offset<br>Full Scale<br>Differential Non-Linearity | <br>0.009<br>0.009<br>0.009 | | | <br>LSB/°C<br>LSB/°C<br>LSB/°C | |
| Off Isolation | | −60 | | dB | 2, 3 |
| Feedthrough | −60 | | | dB | 2 |
| $V_{CC}$ Power Supply Rejection | −60 | | | dB | 2 |
| Input Resistance | | 1K | 5K | Ω | |
| D.C. Input Leakage | | 0 | 3.0 | µA | |
| Sample Time: Prescaler On<br>Prescaler Off | 15<br>8 | | | States<br>States | 4<br>4 |
| Input Capacitance | 3 | | | pF | |

**NOTES:**
*An "LSB", as used here, has a value of approximately 5 mV.
1. Typical values are expected for most devices at 25°C but are not tested or guaranteed.
2. DC to 100 KHz.
3. Multiplexer Break-Before-Make Guaranteed.
4. One state = 167 ns at 12 MHz, 250 ns at 8 MHz.

## A/D GLOSSARY OF TERMS

**ABSOLUTE ERROR**—The maximum difference between corresponding actual and ideal code transitions. Absolute Error accounts for all deviations of an actual converter from an ideal converter.

**ACTUAL CHARACTERISTIC**—The characteristic of an actual converter. The characteristic of a given converter may vary over temperature, supply voltage, and frequency conditions. An actual characteristic rarely has ideal first and last transition locations or ideal code widths. It may even vary over multiple conversions under the same conditions.

**BREAK-BEFORE-MAKE**—The property of multiplexer which guarantees that a previously selected channel will be deselected before a new channel is selected (e.g., the converter will not short inputs together).

**CHANNEL-TO-CHANNEL MATCHING**—The difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions.

**CHARACTERISTIC**—A graph of input voltage versus the resultant output code for an A/D converter. It describes the transfer function of the A/D converter.

**CODE**—The digital value output by the converter.

**CODE TRANSITION**—The point at which the converter changes from an output code of Q, to a code of Q + 1. The input voltage corresponding to a code transition is defined to be that voltage which is equally likely to produce either of two adjacent codes.

**CODE WIDTH**—The voltage corresponding to the difference between two adjacent code transitions.

**D.C. INPUT LEAKAGE**—Leakage current to ground from an analog input pin.

**DIFFERENTIAL NON-LINEARITY**—The difference between the ideal and actual code widths of the terminal based characteristic.

**FEEDTHROUGH**—Attenuation of a voltage applied on the selected channel of the A/D Converter after the sample window closes.

**FULL SCALE ERROR**—The difference between the expected and actual input voltage corresponding to the full scale code transition.

**IDEAL CHARACTERISTIC**—A characteristic with its first code transition at $V_{IN}$ = 0.5 LSB, its last code transition at $V_{IN}$ = ($V_{REF}$ − 1.5 LSB) and all code widths equal to one LSB.

**INPUT RESISTANCE**—The effective series resistance from the analog input pin to the sample capacitor.

**LSB—Least Significant Bit:** The voltage corresponding to the full scale voltage divided by $2^n$, where n is the number of bits of resolution of the converter. For an 8-bit converter with a reference voltage of 5.12V, one LSB is 20 mV. Note that this is different than digital LSBs, since an uncertainty of two LSB, when referring to an A/D converter, equals 40 mV. (This has been confused with an uncertainty of two digital bits, which would mean four counts, or 80 mV.)

**NON-LINEARITY**—The maximum deviation of code transitions of the terminal based characteristic from the corresponding code transitions of the ideal characteristic.

**OFF-ISOLATION**—Attenuation of a voltage applied on a deselected channel of the A/D converter. (Also referred to as Crosstalk.)

**REPEATABILITY**—The difference between corresponding code transitions from different actual characteristics taken from the same converter on the same channel at the same temperature, voltage and frequency conditions.

**RESOLUTION**—The number of input voltage levels that the converter can unambiguously distinguish between. Also defines the number of useful bits of information which the converter can return.

**SAMPLE TIME**—Begins when the sample capacitor is attached to a selected channel and ends when the sample capacitor is disconnected from the selected channel.

**TEMPERATURE COEFFICIENTS**—Change in the stated variable per degree centigrade temperature change. Temperature coefficients are added to the typical values of a specification to see the effect of temperature drift.

**TERMINAL BASED CHARACTERISTIC**—An actual characteristic which has been rotated and translated to remove zero offset and full scale error.

**$V_{CC}$ REJECTION**—Attenuation of noise on the $V_{CC}$ line to the A/D converter.

**ZERO OFFSET**—The difference between the expected and actual input voltage corresponding to the first code transition.

## 80C196KB FUNCTIONAL DEVIATIONS

The 80C196KB has the following problems.

1. The DJNZW instruction is not guaranteed to be functional. The instruction, if encountered, will not cause an unimplemented opcode interrupt. (The opcode for DJNZW is 0E1 Hex.) The DJNZ (byte) instruction works correctly and should be used instead.
2. The CDE function is not guaranteed to work. The CDE pin must be directly connected to $V_{SS}$.
3. The HSI unit has two errata: one dealing with resolution and the other with first entries into the FIFO.

   The HSI resolution is 9 states instead of 8 states. Events on the same line may be lost if they occur faster than once every 9 state times.

   There is a mismatch between the 9 state time HSI resolution and the 8 state time timer. This causes one time value to be unused every 9 timer counts. Events may receive a time-tag one count later than expected because of this "skipped" time value.

   If the first two events into an empty FIFO (not including the Holding Register) occur in the same internal phase, both are recorded with one time-tag. Otherwise, if the second event occurs within 9 states after the first, its time-tag is one count later than the first's. If this is the "skipped" time value, the second event's time-tag is 2 counts later than the first's.

   If the FIFO and Holding Register are empty, the first event will transfer into the Holding Register after 8 state times, leaving the FIFO empty again. If the second event occurs after this time, it will act as a new first event into an empty FIFO.
4. The serial port Framing Error flag fails to indicate an error if the bit preceding the stop bit is a 1. This is the case in both the 8-bit and 9-bit modes. False framing errors are never generated.

## DIFFERENCES BETWEEN THE 80C196KA AND THE 80C196KB

The 8XC196KB is identical to 8XC196KA except for the following differences.

1. ALE is high after reset on the 80C196KB instead of low as on the 80C196KA.
2. The DJNZW instruction is not guaranteed to work on the 80C196KB.
3. The $\overline{HOLD}$/$\overline{HLDA}$ bus protocol is available on the 80C196KB.

## CONVERTING FROM OTHER 8096BH FAMILY PRODUCTS TO THE 80C196KB

The following list of suggestions for designing an 809XBH system will yield a design that is easily converted to the 80C196KB.

1. Do not base critical timing loops on instruction or peripheral execution times.
2. Use equate statements to set all timing parameters, including the baud rate.
3. Do not base hardware timings on CLKOUT or XTAL1. The timings of the 80C196KB are different than those of the 8X9XBH, but they will function with standard ROM/EPROM/Peripheral type memory systems.
4. Make sure all inputs are tied high or low and not left floating.
5. Indexed and indirect operations relative to the stack pointer (SP) work differently on the 80C196KB than on the 8096BH. On the 8096BH, the address is calculated based on the un-updated version of the stack pointer. The 80C196KB uses the updated version. The offset for POP[SP] and POP nn[SP] instructions may need to be changed by a count of 2.
6. The $V_{PD}$ pin on the 8096BH has changed to a $V_{SS}$ pin on the 80C196KB.

T-49-19-16

T-49-19-59

## DATA SHEET REVISION HISTORY

This data sheet is valid for the CPU and ROM devices which have a "B" suffix on the topside tracking number. The 87C196 may or may not have the suffix on the topside number.

This is a new data sheet that integrates the 87C196KB (order number 270590-003) and the 83C196KB/80C196KB (order number 270634-003) data sheets.

The following differences exist between this data sheet (-001) and each of the above mentioned data sheets.

1. The status of the data sheet was upgraded from ADVANCE INFORMATION to PRELIMINARY.
2. The warning about the ABSOLUTE MAXIMUM RATINGS was reworded and a notice of disclaimer was added to the electrical specifications section.
3. $V_{IH2}$ was increased from 2.2V to 2.6V.
4. $I_{IL1}$ was increased from $-950\ \mu A$ to $-1.2$ mA. This change was documented in the previous revision of the data sheets but the D.C. Characteristics table did not reflect the change.
5. Maximum $I_{PD}$ specification was added to the D.C. table and $I_{PD}$ note was deleted.